SLAVE LOGIC ANALYZER
2302-5012-00

July 1981

GenRad/Development Systems Division
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Culver City, CA 90230

REVISION HISTORY

Title	Number	Date	Notes
Slave Logic Analyzer	2302-5012-00	7/81	First Edition

RELATED PUBLICATIONS

Slave Emulator Control Unit Hardware Reference Manual	2302-5000-00

GenRad

PREFACE

This manual introduces and discusses the concepts of Slave Logic Analyzer operation. It prepares the user to install and operate the SLA for debugging prototype system in real time. Special emphasis is given to system commands and console displays. This manual consists of:

Chapter 1, INTRODUCTION, covers the basics of the Slave Logic Analyzer subsystem, specifications, and documentation.

Chapter 2, SERVICE AND MAINTENANCE, describes provisions of customer service and parts information.

Chapter 3, INSTALLATION, discusses Logic Analyzer support and installation.

Chapter 4, OPERATION, narrates the technique of invoking the Slave Logic Analyzer, presents general operation of the system, defines the use of commands, and details the finer points of Logic Analyzer operation.

The information in this manual is subject to change without prior notice.

Please note that a **Documentation Reply Card** is included in this manual. When you complete and return it, you help us produce better documentation for you.

A **User Registration Card** is included in the set of manuals you receive with your GenRad/DSD system. When you complete and return the User Registration Card, you ensure that you will receive all updates and new information for your configuration.

For your convenience, a list of **GenRad/DSD Service Locations** is appended to this manual.

CONTENTS

CONTENTS (Concluded)

ILLUSTRATIONS

ABBREVIATIONS

ABBREVIATION	DEFINITION
ADS	Advanced Development System
ASCII	American Standard Code for Information Interchange
AWG	American Wire Gauge
BCD	Binary Coded Decimal
BP	Breakpoint
BUF	Buffer
CAP	Capacitor
CER	Ceramic
CONN	Connector
CPU	Central Processor Unit
DIP	Dual In-line Package
DR	Driver
DSD	Development Systems Division
EP	Emulator Personality
FF	Flip-Flop
GND	Ground
HEX	Hexadecimal
IC	Integrated Circuit
INV	Inverter
LA	Logic Analyzer
LB/SQ IN.	Pounds Per Square Inch
LED	Light Emitting Diode
MEM	Memory
MOT	Motorola
MUX	Multiplexor
MV	Multivibrator
OCTD	Octal
OSC	Oscillator
POS	Positive
PROM	Programmable Read Only Memory
PWB	Printed Wiring Board
RAM	Random Access Memory
REC	Receiver
RIB	Ribbon
ROM	Read-Only Memory
SEL	Select
SIP	Single-In-Line Package
SLA	Slave Logic Analyzer
SPR	Sprague
ST	State
TANT	Tantalum
TI	Texas Instruments

CHAPTER 1

INTRODUCTION

1.1 PURPOSE AND SCOPE

The purpose of this manual is to inform and instruct the user specifically about the Logic Analyzer portion of the Slave Emulator. The depth of coverage is sufficient for the intended purpose. This manual has been prepared assuming the user has a knowledge of GenRad Advanced Development System operation, including the Slave Emulator.

1.2 SLA OVERVIEW

The SLA simplifies debugging and troubleshooting tasks by displaying detailed pictures of time-related events within digital circuits. This allows the user to view bus data during program execution.

The SLA has a sampling rate of 10MHz. Information is recorded synchronously with the system, and stored in an area of memory contained in the SLA hardware.

The SLA samples and stores a maximum of 256 traces for up to 24 address lines, up to 16 data lines, four external user-defined lines, and 20 processor-dependent lines. A hardware register (Trace Qualifier) selects the trace to be stored in SLA memory.

These and other details are explained in **Chapter 4, OPERATION.**

1.3 SLA SUBSYSTEM DESCRIPTION

The SLA subsystem consists of one 2302-4746-01 Logic Analyzer card and one 2302-0234-01 Cable Assembly for Internal LA-P3 to EP-P3 connection.

1.3.1 THE SLA CARD

The Logic Analyzer is a standard Slave Emulator card with two rear double-sided edge connectors, P3 and P5, for interfacing the Breakpoint and Emulator personality cards. The front edge connectors, P1 and P2, plug into the motherboard (backplane). P1 and P2 are identical on all Emulator cards. There are approximately 122 components on this card, containing 256x4 RAMs, assorted IC logic arrays, resistor PAKs, a 20MHz crystal oscillator, capacitors and resistors.

1.3.2 SLA CARD DIGEST

The SLA card records bus signals during emulation, beginning at a specific event which is predetermined on the breakpoint card. The SLA 24-bit cycle counter records the time (or bus cycle) between two events. These two events are detected by Breakpoints 1 and 2. Breakpoint 1 starts the count and Breakpoint 2 ends the count. The SLA card records specified bus cycles determined by the trace qualifier.

The SLA block diagram is shown in **Figure 1-1.** Notice that memory logic falls into two groups:

(1) main memory and (2) memory address counters. Traces are stored in sixteen 256 x 4-bit main memory RAMs. Information to be stored can be restricted to a READ or WRITE to a specified location. The memory addresses are two 4-bit synchronous counters for addresses A0 through A7.

Data latches coming off the bus consist of 24 address lines (BA0-BA23), 16 data lines (BD0-BD15), and four control lines (X6, R/W-, X17, and BHE). Non-bus signals are 16 processor-dependent inputs (X0-X15) and four external conditions (EC0-EC3).

The timing logic consists of a 20MHz crystal clock source and a 10/1MHz real-time clock, a clock selector, and a 24-bit cycle counter working into the bus through a buffer array carrying BD0-BD7.

NOTE

Symbols inside blocks refer to IC DIPS on Schematic, Logic Analyzer, 2302-4746. For example, U4, U5, U6, U38-42 are data latches.

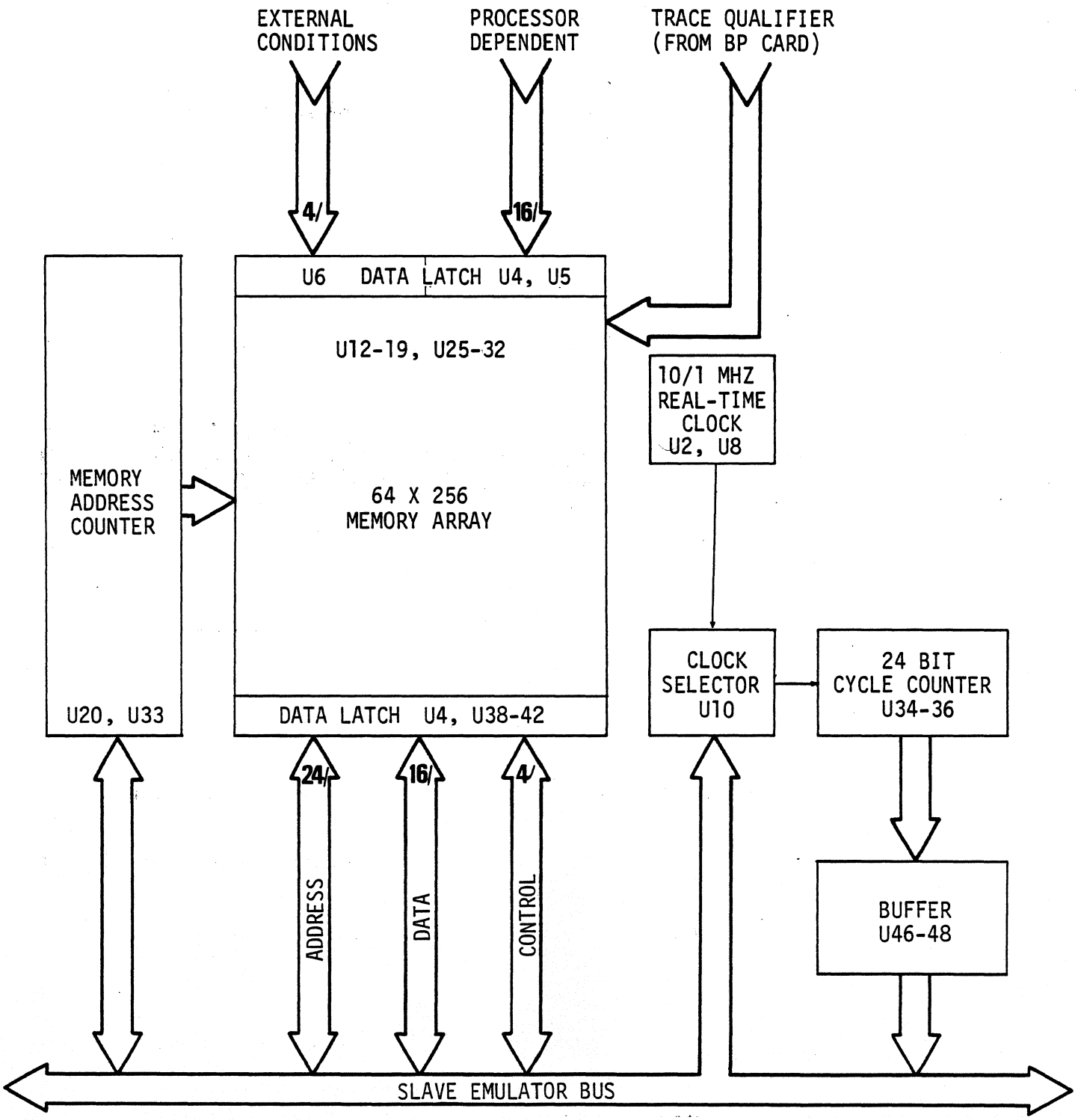


Figure 1-1. Logic Analyzer Block Diagram

1.4 SPECIFICATIONS

1.4.1 THE SLA CARD

Width:	9 inches (23 cm)
Length:	12 inches (30 cm)
Thickness:	.06 inches (1-1/2 mm)
Weight:	8 oz. (226.8 grams)

1.4.2 CABLE ASSEMBLY, INTERNAL (LA-P3 TO EP-P3)

Overall Length:	3.25 inches (8 cm)

CHAPTER 2

SERVICE AND MAINTENANCE

2.1 CUSTOMER SERVICE

Our warranty (at the front of this manual) refers to the materials and workmanship of our product. If a malfunction occurs, our service engineers will assist in any way possible. If the difficulty cannot be eliminated by use of the following service instructions, please write or phone the nearest GenRad/DSD service facility, giving full information about the trouble and the steps taken to remedy it. Describe the instrument by name, catalog number, serial number, and ID lot number if any. (Refer to front and rear panels.)

2.2 INSTRUMENT RETURN

2.2.1 RETURNED MATERIAL NUMBER

Before returning an instrument to a GenRad/DSD facility for service, please ask our nearest office for a "Returned Material" number. Use of this number in correspondence and on a tag tied to the instrument will insure proper handling and identification. After the initial warranty period, please avoid unnecessary delay by sending a purchase order number.

2.2.2 PACKAGING

To safeguard your instrument during shipment, please use packaging that is adequate to protect it from damage during shipment. Use of the original packaging is preferable. Any GenRad/DSD field office may advise or provide packing material for this purpose. Contract packaging companies in many cities provide dependable custom packaging on short notice. The three recommended packaging methods are:

a. Rubberized Hair
b. Excelsior
c. Bubble Pack

a. Rubberized Hair. Cover painted surfaces of instrument with protective wrapping paper. Pack instrument securely in strong protective corrugated container (350 lb/sq. in., bursting test), with 2-inch rubberized hair pads placed along all surfaces of the instrument. Insert fillers between pads and container to ensure a snug fit. Mark the box "Delicate Instrument" and seal with strong tape or metal bands.

b. Excelsior. Cover painted surfaces of instrument with protective wrapping paper. Pack instrument in strong corrugated container (350 lb/sq. in., bursting test), with a layer of excelsior about six inches thick packed firmly against all surfaces of the instrument. Mark the box "Delicate Instrument" and seal with strong tape or metal bands.

c. Bubble Pack. Bubble packs are continuous thin sheets of clear double sealed plastic material with bulging air bubbles spaced along the sheet to act as cushions. Cover painted surfaces of instrument with protective wrapping paper. Pack instrument in strong corrugated container (350 lb/sq. in., bursting test), with several layers of bubble pack wrapped firmly against all surfaces of the instrument. Mark the box "Delicate Instrument" and seal with strong tape or metal bands.

2.3 PARTS LIST

These parts lists are only for the Logic Analyzer card and Internal Cable Assembly. When ordering parts, use the full description.

PARTS LIST
LOGIC ANALYZER 2302-4746-01

ITEM	PART NO.	QTY	DESCRIPTION	MFR	MFR PART NO.	SYMBOL
1	2302-0746-01	1	PWB, LOGIC ANALYZER			
2	5431-8600-00	2	IC, 4/2-IN POS NAND	TI	SN74LS00N	U3,24
3	5431-8761-00	1	IC, BINARY 4-BIT COUNT	TI	SN74LS161AN	U7
4	5431-8630-00	1	IC, 8-IN POS NAND	TI	SN74LS30N	U49
5	5431-8632-00	1	IC, 4/2-IN POS OR	TI	SN74LS32N	U37
6	5431-8674-00	1	IC, 2/D-FLIP-FLOP	TI	SN74LS74AN	U8
7	5431-8686-00	1	IC, 4/X-OR GATES	TI	SN74LS86N	U11
8	5431-8707-00	1	IC, 2/JK FLIP-FLOP	TI	SN74LS107N	U23
9	5431-8738-00	2	IC, 3-8 LINE DECODER	TI	SN74LS138N	U21,22
10	5431-8751-00	1	IC, 1 of 8 DATA SEL/MUX	TI	SN74LS151N	U10
11	5431-8761-00	2	IC, BINARY 4-BIT COUNT	TI	SN74LS161N	U33,20
12	5431-8775-00	1	IC, 4/D-FLIP-FLOP	TI	SN74LS175N	U44
13	5431-8844-00	4	IC, 8/BUF-DRIVE-REC	TI	SN74LS244N	U43,46,47,48
14	5431-8968-00	1	IC, 6/3-STATE INVERTER	TI	SN74LS368N	U9
15	5431-8974-00	8	IC, 8/D-FLIP-FLOP	TI	SN74LS374N	U38-42,4-6
16	5431-8993-00	3	IC, 2/4-BIT BINARY COUNT	TI	SN74LS393N	U34-36
17	5627-1017-00	16	IC, RAM BIPOLAR 256x4	FC	93L422	U12-19,25-32
18	7540-1816-00	1	SOCKET, IC 16-PIN	TI	C-9316-02	TCI
19	5434-0206-00	1	OSC, 20 MHZ, 14-PIN DIP	MOT	K1100A-20.MHZ	U2
20	6099-2105-00	7	RES, 1K, 1/4W, 5%	A-B	RC0G7GF102J	R1-7
21	6740-2663-00	1	RES,PAK,9/4.7K,10-PINSIP	CTS	750-101-R4.7K	RP1
22	4431-4103-00	57	CAP, IC 01mf, 50V	AVX	MD015E103ZAA	C8-64
23	4450-6260-00	7	CAP, 33mf, TANT, 10V	SPR	196D336X9010KA1	C1-7

PARTS LIST
CABLE ASSEMBLY INTERNAL LA-P3 TO EP-P3

ITEM	PART NO.	QTY	DESCRIPTION	SYMBOL
1	4230-4751-00	2	CONN CARD EDGE, 26 CONTACT	EP-P3,LA-P3
2	0034-6938-00	1	CABLE, RIB 26 CONDUCTOR, 28 AWG	

2.4 IC INFORMATION

The integrated circuits used in the SLA logic are mostly all low-power Schottky TTL's. Notice that the total number of pins per DIP are either 14, 16, 20, or 22.

TYPE	LOGIC DESCRIPTION	PIN NUMBER	
		GND	Vcc
74LS00	4/2-IN POS NAND	7	14
74LS161	BINARY 4-BIT COUNT	8	16
74LS30	8-IN POS NAND	7	14
74LS32	4/2-IN POS OR	7	14
74LS74	2/D - FF	7	14
74LS86	4/X - OR	7	14
74LS107	2/JK FF	8	16
74LS138	3-8 LINE DECODER	8	16
74LS151	1 OF 8 DATA SEL/MUX	8	16
74LS161	4-BIT BINARY COUNTER	8	16
74LS175	4/D - FF	8	16
74LS244	8/BUF-DR REC	10	20
74LS368	6/3-STATE INV	8	16
74LS374	8/D - FF	10	20
74LS393	2/4-BIT BINARY COUNTER	7	14
93L422	256x4 BIPOLAR RAM	8	22
74S289	64-BIT RAM	8	16
74S08	2-IN POS AND	7	14
74S02	2-IN POS NOR	7	14
74S03	2-IN POS NAND O/C	7	14
7404	HEX INV	7	14
74221	MONOSTABLE MV	8	16
74LS04	HEX INV	7	14
74LS08	2-IN NAND	7	14
74LS10	3-IN NAND	7	14
74LS30	8-IN NAND	7	14
74LS157	2 TO 1 SEL/MUX	8	16
74LS373	OCTD LATCH	10	20
8098	BUS DR INV, 3-ST	8	16

2.5 MNEMONIC DESCRIPTIONS

The following signal names were taken from the SLA schematic diagrams included in this manual. Most of the signals are those which traverse the bus. In other words, these signals go off the card. A signal which stays on the card is shown by an asterisk after its name. See notes.

MNEMONIC	LOGIC ANALYZER
LAS-	Logic Analyzer Strobe
BA0-BA24	Bus Address, 0-24
BD0-BD14	Bus Data, 0-14
BHE+	Byte, High Enable
EPCYC-	Emulation Processor Cycle
PRTY-	Priority Error Input
MEM-	Memory Cycle
IPWAIT-	Interface Processor Wait
RFSH-	Refresh Cycle
BYTE+	Byte - 8-Bit Operation
R/W-	Read Write Cycle
HLDA-	Hold Acknowledge
MRDY+	Memory Ready
(SA0+)-(SA2+)	System Address, 0-2
(BP1+)-(BP3+)	Breakpoint, 1-3
BP1OUT-	Breakpoint 1, Out
EPI-	Emulation Processor Interrupt
MAP-	Memory Mapper - Internal/External
TIME-	Test Memory Enable
SYS+	System Address Enable
BP2OUT-	Breakpoint 2, Output
BP1IN-BP2IN	Breakpoint 1-2, Input
IO0-IO31	Input/Output, 0-31
(SA1+)-(SA3+)	System Address, 1-3
BP2+	Breakpoint 2
BP4+	Breakpoint 4
LAI-	Logic Analyzer Interrupt
WPROUT-	Write-Protect
BP3OUT-	Breakpoint 3, OUT
RSTPB-	Reset Push Button
BP3IN-	Breakpoint 3, IN
BP4OUT-	Breakpoint, OUT

NOTES: (1) - means Active Low Bus Signals
(2) + means Active High Bus Signals
(3) * means Active Low Non-Bus Signals

2.5 Continued

MNEMONIC	LOGIC ANALYZER
BP4IN-	Breakpoint, IN
X0-X15	Processor-dependent Logic Analyzer inputs
EC0-EC3	"External Condition" 0-3
TQ	Trace Qualifier for Logic Analyzer
BP2-	Breakpoint 2
BP3-	Breakpoint 3
D0-D7	Slave Emulator Bus Data, 0-7
CLRCNT*	Clear address counter overflow bit.
CYCCNT	"Cycle Count" Enable counting of Breakpoint 3 cycling.
DATA STR	Inverse of Logic Analyzer Strobe (LAS)
SELL*	Select read-data buffer for Logic Analyzer RAMS.
SELR*	Enable Sell*

NOTES: (1) - means Active Low Bus Signals
(2) + means Active High Bus Signals
(3) * means Active Low Non-Bus Signals

2.6 LOGIC SCHEMATICS

The Logic Analyzer schematic, 2302-4746-01-SD, consists of five sheets. Sheets 1 and 2 depict reference information, such as pin number and signal name, for Edge Connectors P1, P2, P3, and P5. This information can be traced to logic inputs and outputs on the remaining sheets. Each IC DIP is labeled with pin numbers, symbol, and I/O signals.

Figure 2-1 shows a section of logic extracted from Sheet 3. The bow-tie connector symbol represents bi-directional bus signal flow. The number 1, within the left side of the bow-tie means P1. To the left of this number are the numbers A31, B31, A30, B30, A29, B29, A28, and B28. "A" stands for the upper or component side of the PWB, while "B" stands for the other side. The two-digit numbers are the pin numbers. Therefore, A31 means P1 pin 31.

BD0 through BD7 are mnemonics for 8-bit bus data on lines 0 through 7. The symbols in parentheses are schematic page numbers and zone location on that page. For example, (4-D2) means page 4, zone D2.

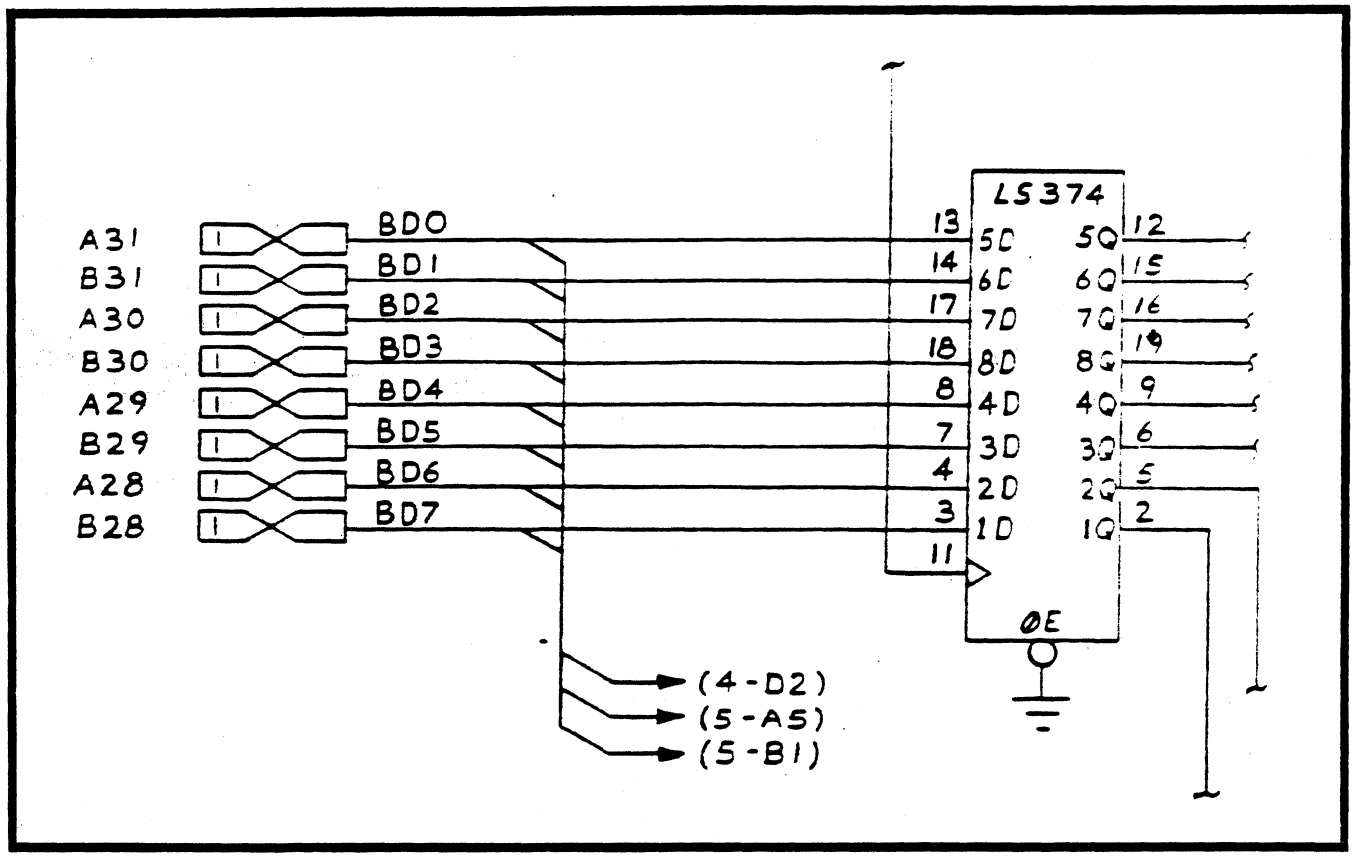
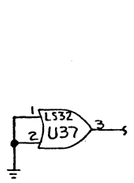
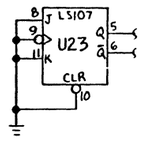
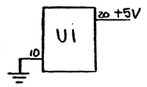


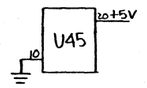
Figure 2-1. Logic Schematic Section

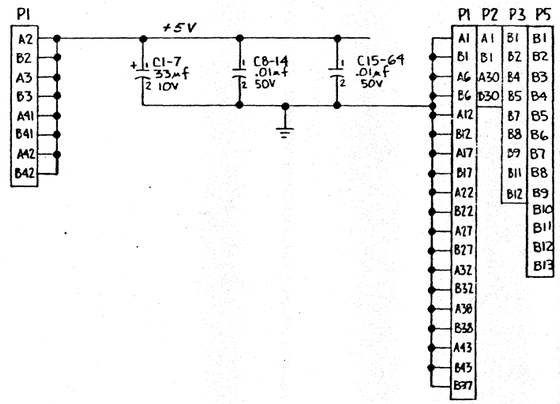
SPARES











COMPONENT	VCC	GND
U2,U3,U8,U11,U23,U29, U34-37, U49	14	7
U7,U9,U10,U20-22, U33,U44	16	8
U4-6, U38-43, U46-48 U1 (SPARE) U45 (SPARE)	20	10
U12-19, U25-32	22	8

1. C1-C6 AND C8-C13 CAP PAIRS TO BE MOUNTED ON THE NON-CONNECTOR SIDES OF THE BOARD, EQUALLY SPACED WITH 3 PAIRS TO A SIDE. C7 AND C14 PAIR TO BE MOUNTED NEAR I/O PINS P1A-43 & P1B-43. REST OF CAPS, 1 PER IC. LOCATION.

NOTES: UNLESS OTHERWISE SPECIFIED

APPROVAL	DATE
DRWN: CAZ	2-10-81
CK:	
ENG:	4/21/81
ENG:	4/21

X4 INCORP ECO 1654	CAZ	4/30/81
X3 INCORP ECO 1631	CAZ	4/20/81
X2 PILOT REL 1604	CAZ	4/3/81
X2: INC. EDC 131-96	JT	3-5-81
X1: INC. EDC 122-06	JT	2-24-81
X0: INITIAL DRAW	JT	2-10-81

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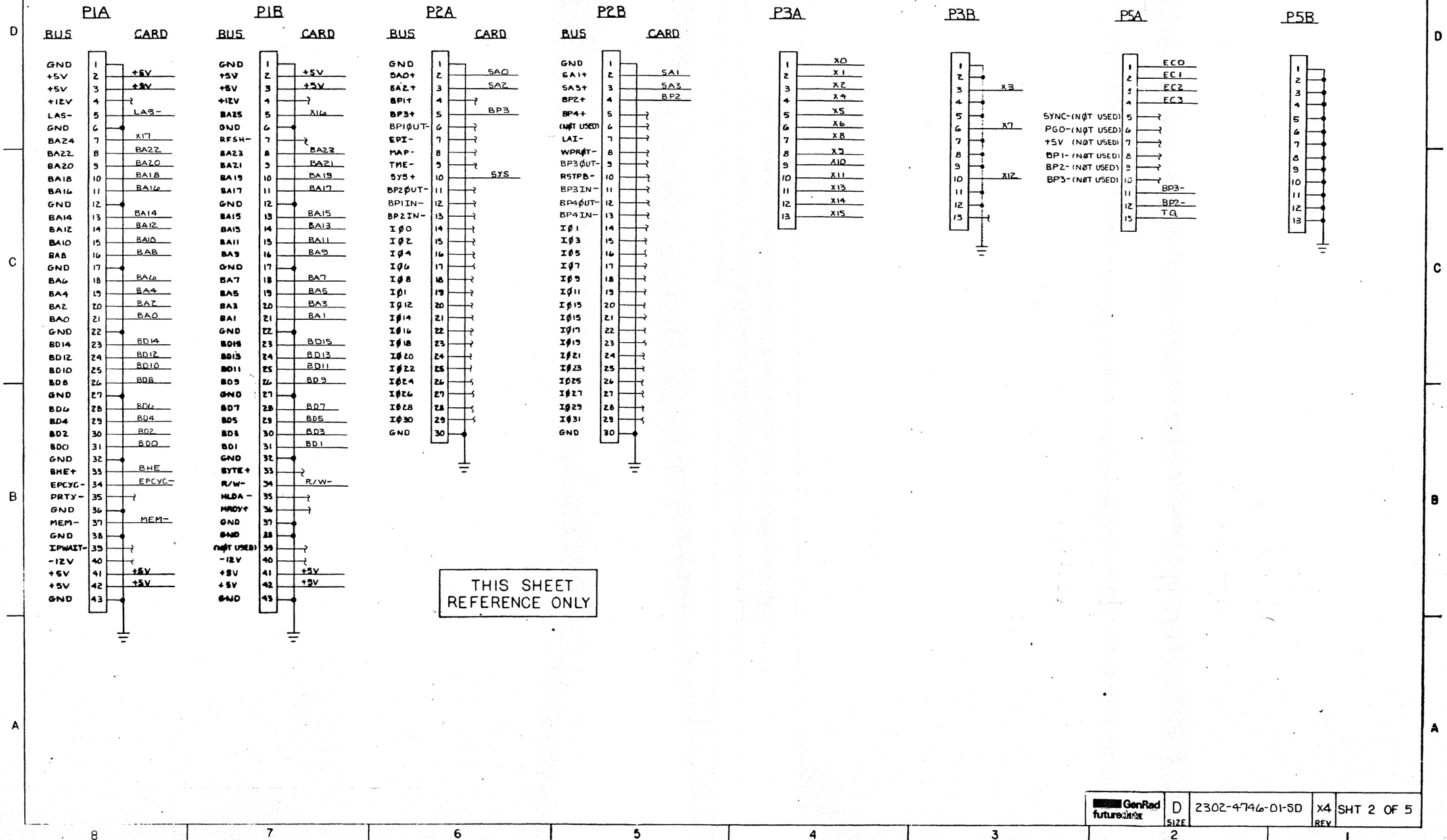
SCHEMATIC, LOGIC ANALYZER

D 2302-4746-01-SD X4 SH 1 OF 5


P1A
BUS
CARD
GND 1
+5V 2
+5V 3
+12V 4
LAS- 5
GND 6
BAZ4 7
BAZZ 8
BAZO 9
BA18 10
BA16 11
GND 12
BA14 13
BAIZ 14
BAIO 15
BA8 16
GND 17
BA6 18
BA4 19
BAZ 20
BAO 21
GND 22
BD14 23
BD12 24
BD10 25
BD8 26
GND 27
BD6 28
BD4 29
BD2 30
BDO 31
GND 32
BHE+ 33
EPCYC- 34
PRTY- 35
GND 36
MEM- 37
GND 38
IPWAIT- 39
-12V 40
+5V 41
+5V 42
GND 43
+5V
+5V
LAS-
X16
X17
BAZZ
BAZO
BA18
BA16
BA14
BAIZ
BAIO
BA8
BA6
BA4
BAZ
BAO
BD14
BD12
BD10
BD8
BD6
BD4
BD2
BDO
BHE
EPCYC-
MEM-
+5V
+5V
P1B
BUS
CARD
GND 1
+5V 2
+5V 3
+12V 4
BA25 5
GND 6
RFSH- 7
BA23 8
BAZI 9
BA19 10
BAI7 11
GND 12
BA15 13
BAI3 14
BAII 15
BA9 16
GND 17
BA7 18
BA5 19
BA3 20
BAI 21
GND 22
BD15 23
BD13 24
BDII 25
BD9 26
GND 27
BD7 28
BD5 29
BD3 30
BDI 31
GND 32
BYTE+ 33
R/W- 34
HLDA- 35
HRDY+ 36
GND 37
GND 38
(NOT USED) 39
-12V 40
+5V 41
+5V 42
GND 43
+5V
+5V
X16
BA23
BAZI
BA19
BAI7
BA15
BAI3
BAII
BA9
BA7
BA5
BA3
BAI
BD15
BD13
BDII
BD9
BD7
BD5
BD3
BDI
R/W-
P2A
BUS
CARD
GND 1
BA0+ 2
BA2+ 3
BPI+ 4
BP3+ 5
BPIØUT- 6
EPI- 7
MAP- 8
TME- 9
5Y5+ 10
BP2ØUT- 11
BPIIN- 12
BP2IN- 13
IØ0 14
IØ2 15
IØ4 16
IØ6 17
IØ8 18
IØI 19
IØI2 20
IØI4 21
IØI6 22
IØI8 23
IØ20 24
IØ22 25
IØ24 26
IØ26 27
IØ28 28
IØ30 29
GND 30
BA0
BA2
BP3
5Y5
P2B
BUS
CARD
GND 1
BA1+ 2
BA3+ 3
BP2+ 4
BP4+ 5
(NOT USED) 6
LAI- 7
WPRØT- 8
BP3ØUT- 9
RSTPB- 10
BP3IN- 11
BP4ØUT- 12
BP4IN- 13
IØI 14
IØ3 15
IØ5 16
IØ7 17
IØ9 18
IØII 19
IØI3 20
IØI5 21
IØI7 22
IØI9 23
IØ2I 24
IØ23 25
IØ25 26
IØ27 27
IØ29 28
IØ3I 29
GND 30
BA1
BA3
BP2
P3A
1 X0
2 X1
3 X2
4 X4
5 X5
6 X6
7 X8
8 X9
9 X10
10 X11
11 X13
12 X14
13 X15
P3B
1
2
3 X3
4
5
6 X7
7
8
9
10 X12
11
12
13
P5A
1 ECO
2 EC1
3 EC2
4 EC3
5 SYNC-(NØT USED)
6 PGO-(NØT USED)
7 +5V (NØT USED)
8 BP1-(NØT USED)
9 BP2-(NØT USED)
10 BP3-(NØT USED)
11 BP3-
12 BP2-
13 TG
P5B
1
2
3
4
5
6
7
8
9
10
11
12
13
THIS SHEET
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futuredata
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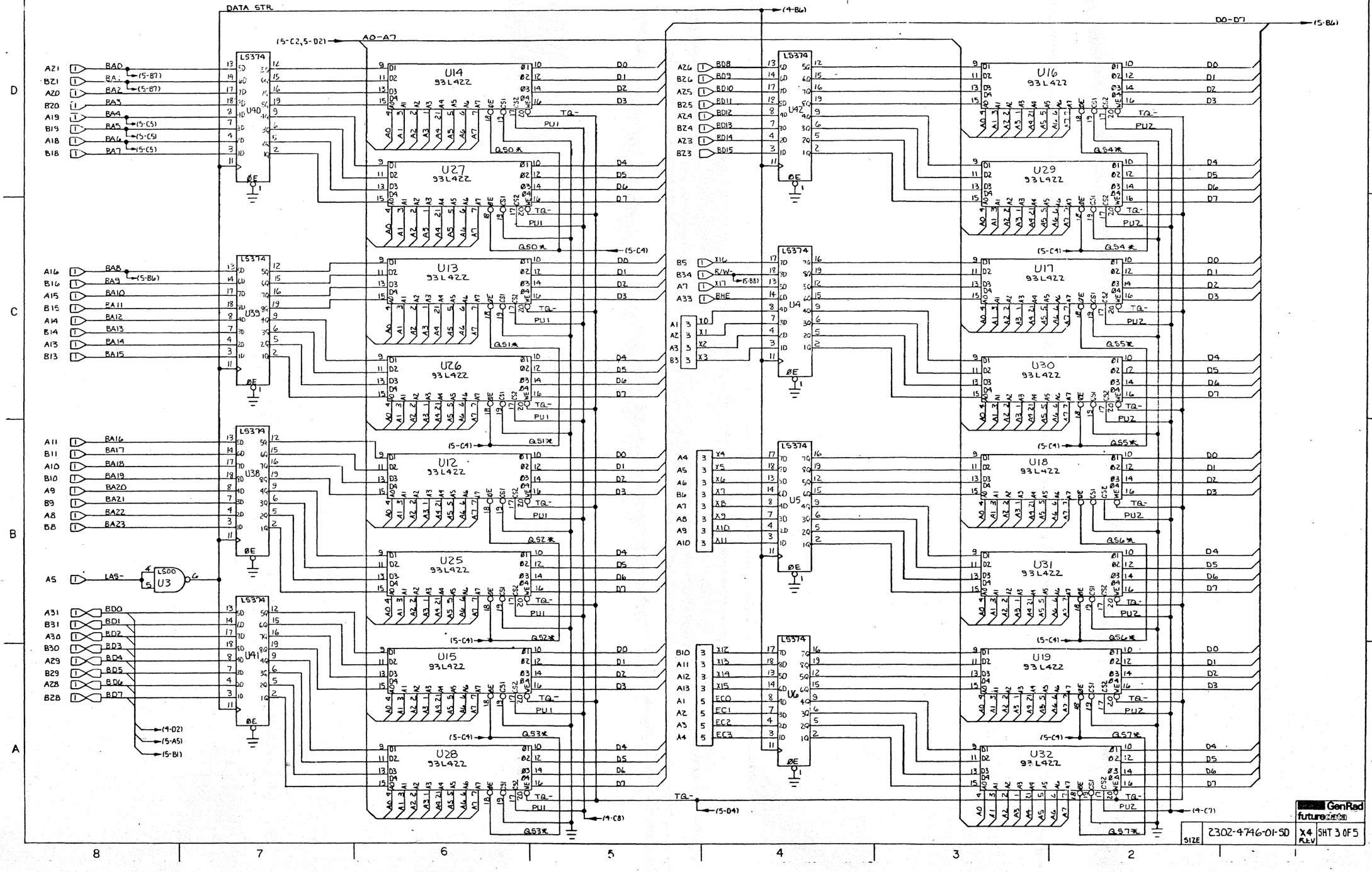
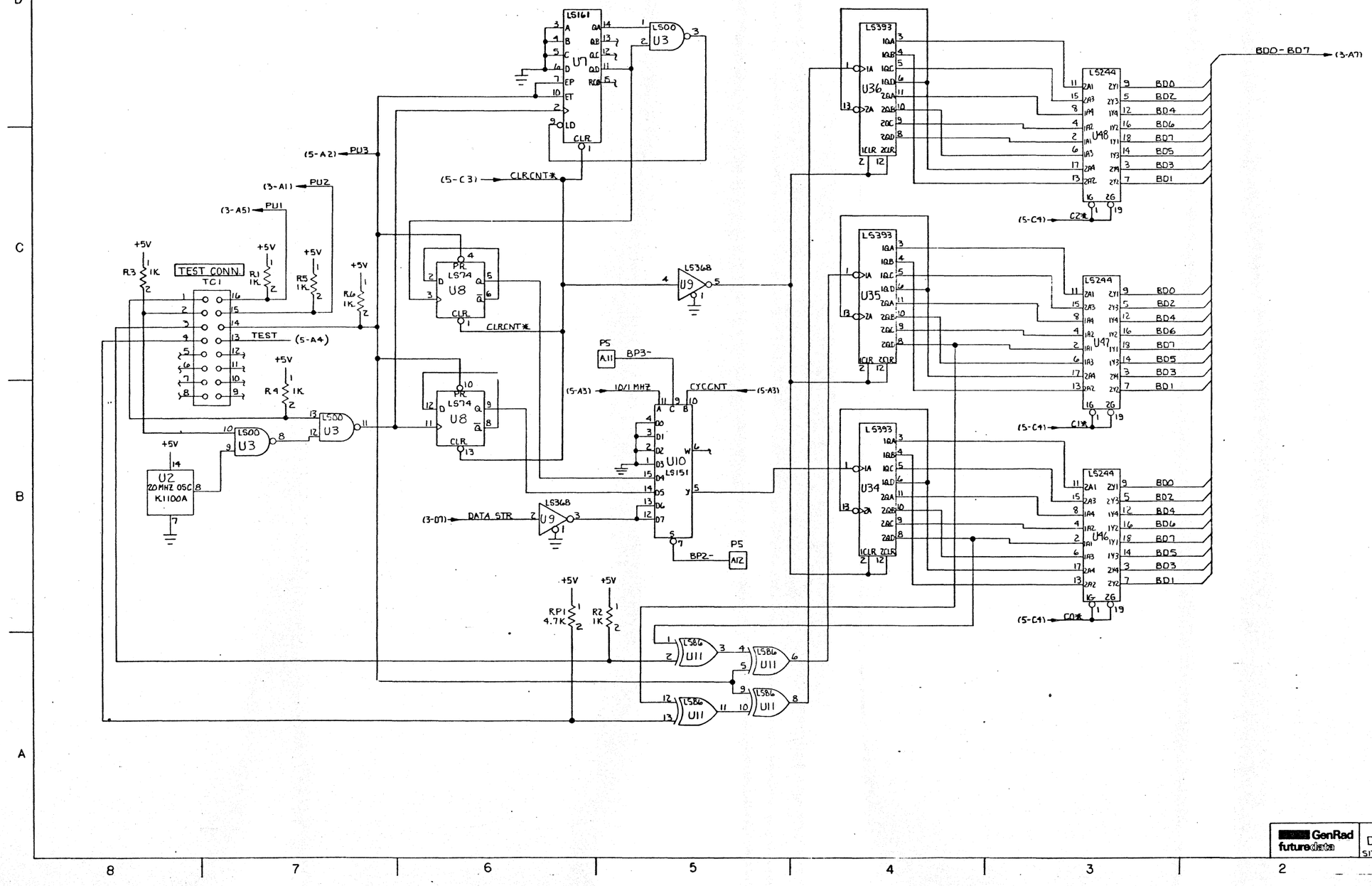
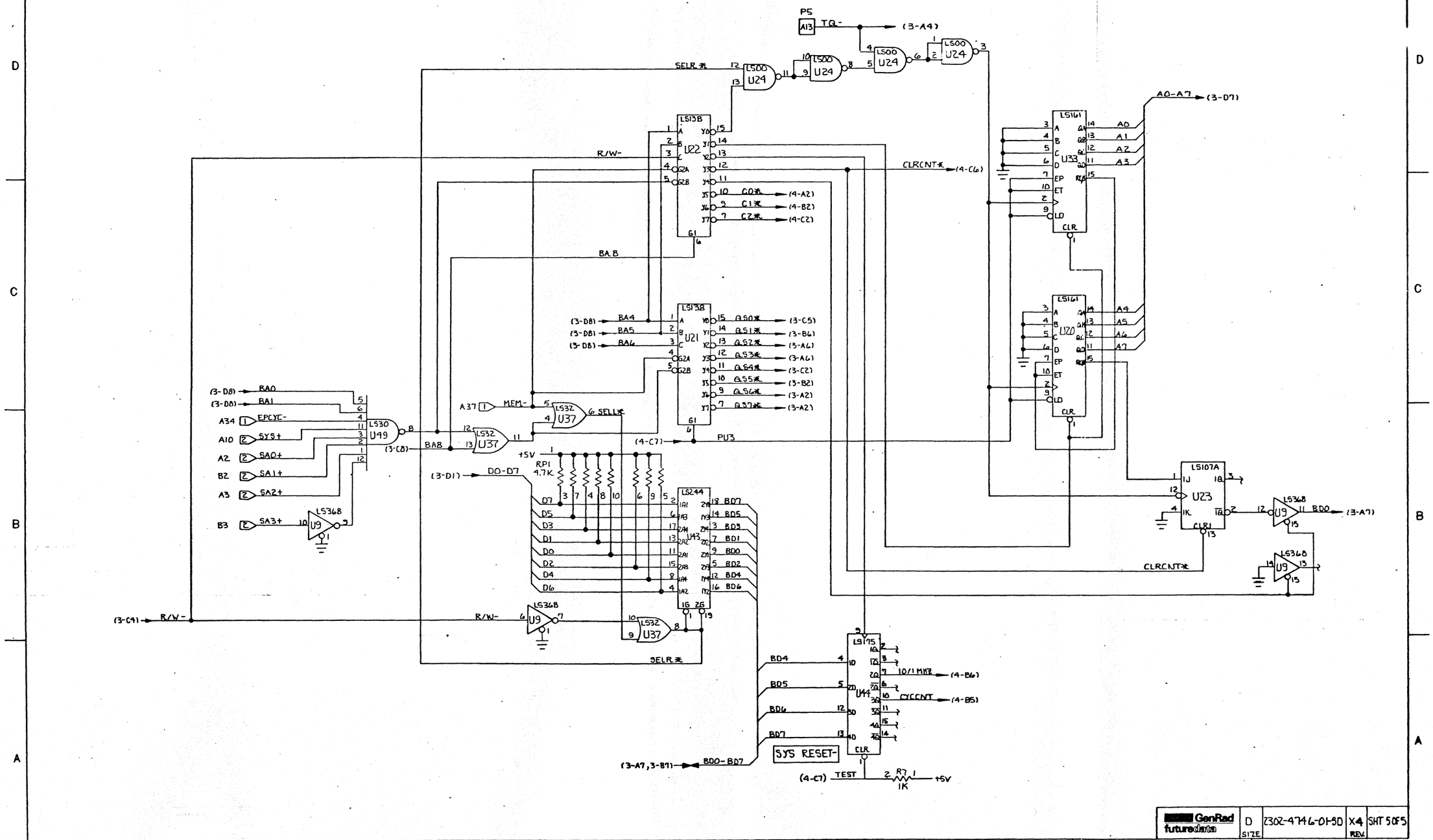
SIZE
2302-4746-01-5D
X4
REV
SHT 2 OF 5


DATA STR
(5-C2,5-D2)
A0-A7
(4-B6)
D0-D7
(5-B6)
LS374
U40
U41
U38
U33
U42
U4
U5
U6
93L422
U14
U27
U13
U26
U12
U25
U15
U28
U16
U29
U17
U30
U18
U31
U19
U32
LS00
U3
BA0
BA1
BA2
BA3
BA4
BA5
BA6
BA7
BA8
BA9
BA10
BA11
BA12
BA13
BA14
BA15
BA16
BA17
BA18
BA19
BA20
BA21
BA22
BA23
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
LAS-
R/W-
BHE
TQ-
PU1
PU2
Q50*
Q51*
Q52*
Q53*
Q54*
Q55*
Q56*
Q57*
(5-C1)
(5-B1)
(5-B7)
(5-C5)
(5-B8)
(9-D2)
(5-A5)
(5-B1)
(9-C8)
(5-D4)
(9-C7)
GenRad
futurenet
SIZE
2302-4746-01-SD
X4 REV
SHT 3 OF 5


LS161
U7
LS00
U3
LS393
U36
LS244
U48
BD0-BD7
(3-A7)
BD0
BD2
BD4
BD6
BD7
BD5
BD3
BD1
(5-C4) C2*
(5-C4) C1*
(5-C4) C0*
U35
U47
U34
U46
LS368
U9
LS74
U8
CLRCNT*
(5-C3) CLRCNT*
(5-A2) PU3
(3-A1) PU2
(3-A5) PU1
TEST CONN.
TC1
TEST
(5-A4)
R3 1K
R1 1K
R5 1K
R6 1K
R4 1K
+5V
U2
20 MHZ OSC
K1100A
PS
A11
BP3-
(5-A3) 10/1 MHZ
CYCCNT
(5-A3)
LS151
U10
BP2-
A12
P5
(3-D7) DATA STR
RP1 4.7K
R2 1K
LS86
U11
GenRad futuredata
D
SIZE
2302-9746-01-SD
X4
REV
SHT 4 OF 5


P5
A13
TQ-
(3-A9)
SELR*
R/W-
BA8
CLRCNT*
(4-C6)
A0-A7
(3-D7)
(3-D8)
BA0
BA1
BA4
BA5
BA6
A34
EPCYC-
A10
SYS+
A2
SA0+
B2
SA1+
A3
SA2+
B3
SA3+
A37
MEM-
SELL*
BAB
(3-C8)
(4-C7)
PU3
+5V
RP1
4.7K
(3-D1)
D0-D7
(3-C9)
R/W-
BD4
BD5
BD6
BD7
BD0-BD7
(3-A7,3-B7)
SYS RESET-
(4-C7)
TEST
R7
1K
10/1 MHZ
(4-B6)
CYCCNT
(4-B5)
BD0
(3-A7)
CLRCNT*
U22
U21
U20
U33
U37
U49
U9
U23
U43
U44
LS138
LS161
LS244
LS175
LS107A
LS368
LS32
LS00
LS30
GenRad
futuredata
D
SIZE
2302-4746-01-00
X4
REV
SHT 5 OF 5

2.7 ASSEMBLY DIAGRAMS

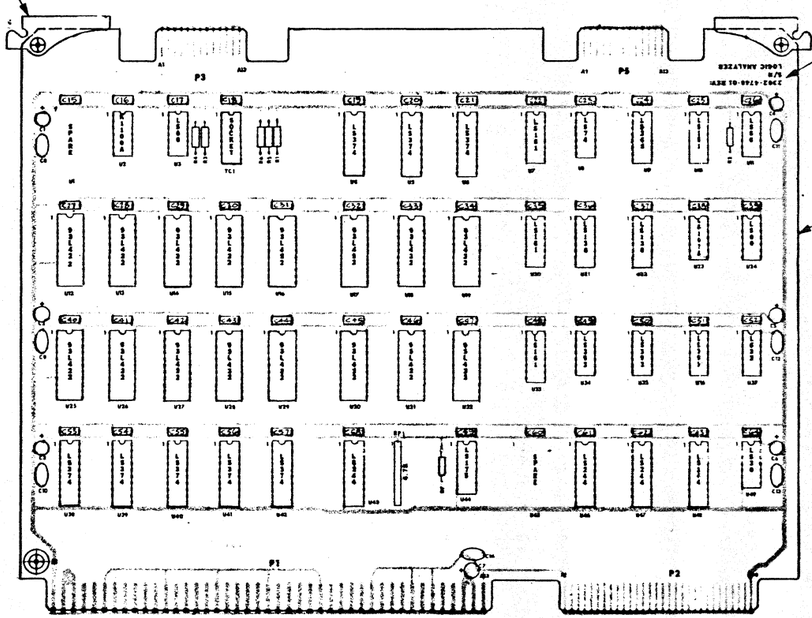
The following assembly diagrams are for the SLA card and the internal LA-P3 to EP-P3 cable.

REVISIONS						
LAL	REV	ECO	DESCRIPTION	DR CH	DATE	APPROVED
	X2	1604	PILOT RELEASE			
	X3	1631	INCORP ECO			
	X4	654	INCORP ECO			

2PL (37)

(1)

(1)



COMPONENT SIDE

2. LEAD PROTRUSION ON SOLDER SIDE TO BE .06 MAX.

(1) MARK ASSEMBLY NO. LATEST REV LEVEL AND SERIAL NO.

NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED	DRAWN BY	DATE 4-81	CHECKED BY	DATE 4-81
DIMENSIONS ARE IN INCHES & APPLY AFTER PLATING. BREAK ALL SHARP EDGES. DECIMAL ANGULAR 2 PLACES ±. ± 3 PLACES ±.	APPROVAL			
MATL:	NAME	SIGNATURE	DATE	
FINISH:	DESIGNER			
	ENGINEER P. FRANCESCHINI		4/30/81	
	PROJECT MGR. J.W. SPANIOL		4/30/81	

GenRad futuredata CULVER CITY CA

TITLE
ASSEMBLY
LOGIC ANALYZER

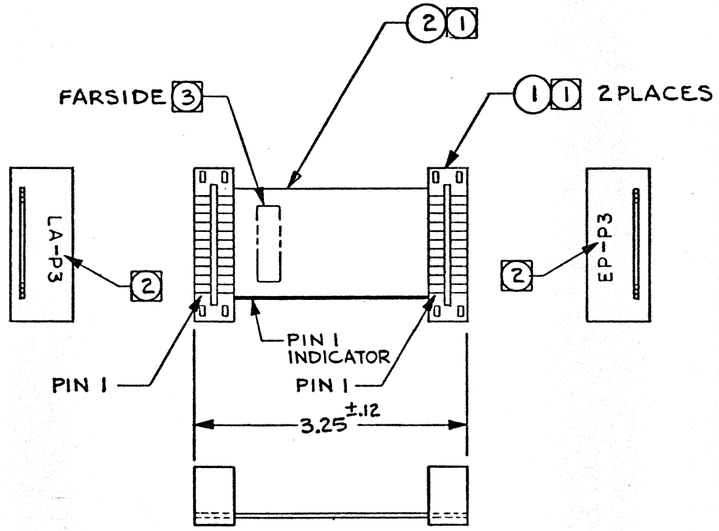
SIZE	DWG. NO.	REV.
D	2302-4746-01-AD	X4

SCALE 1/1 | DO NOT SCALE DRAWING | SHT. 1 OF 2

2302-4746-01-AD | X4

DIETZGEN-POST CLEARPRINT

REVISIONS						
LAL	REV	ECO	DESCRIPTION	DR/CH	DATE	APPROVED
	A0	1542	PROD RELEASE	2/21/81	3/5/81	



SEE SEPARATE PARTS LIST 2302-0234-01-PL

3. RUBBER STAMP ASSY NO., DASH NO., AND CURRENT REV LETTER USING BLACK PERMANENT INK, WITH .12 HIGH CHARACTERS, LOCATED APPROX WHERE SHOWN
2. MARK REF DESIGNATOR USING BLACK PERMANENT INK, WITH .12 HIGH CHARACTERS LOCATED APPROX WHERE SHOWN
1. CRIMP CONNECTORS ONTO CABLE PER MFR'S RECOMENDATIONS.

NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED	DRAWN BY	DATE	CHECKED BY	DATE
DIMENSIONS ARE IN INCHES & APPLY AFTER PLATING. BREAK ALL SHARP EDGES. DECIMAL ANGULAR 2 PLACES ±.— ±— 3 PLACES ±.—		2/19/81		3/5/81
MATL:	APPROVAL			
FINISH:	NAME	SIGNATURE		DATE
	DESIGNER			
	ENGINEER R.J. Leiter			3/5/81
	PROJECT MGR			

GenRad futuredata CULVER CITY CA

TITLE: CABLE ASSY, INTERNAL LA-P3 TO EP-P3

SIZE	DWG. NO.	REV.
C	2302-0234-01-SA	A0

SCALE 1/1 | DO NOT SCALE DRAWING | SHT. 1 OF 1

2302-0234-1

DIETERICH-POST CLEARPRINT

Chapter 3

INSTALLATION

3.1 PREPARATION

Before installing the SLA subsystem, check with your GenRad/DSD service facility to verify that your Slave Emulator is configured with the latest version of:

a. Software
b. Breakpoint Card
c. Interface Processor Card with correct ROM
d. External Probe

> NOTE
>
> All Slave Emulators shipped from GenRad/DSD after April 30, 1981 are correctly configured to operate with the SLA subsystem.

3.2 INSTALLING THE SLA SUBSYSTEM

a. On the Emulator, set the ON/OFF power switch to OFF and remove the a.c. power cord from the rear panel socket.

b. Remove the rear panel.

c. Refer to **Figure 3-1.** Insert the Logic Analyzer card in Position 1 in the card cage.

d. Connect one end of the short flat cable, 2302-0234-01, to the Logic Analyzer card (P3); and the other end of the cable to Personality Card P3.

e. On Cable 2302-0225-01, connect the LA-P5 plug to the Logic Analyzer card.

f. Before replacing the rear panel, make sure that all cables are properly aligned and pushed all the way onto the card edge connectors. Replace the rear panel.

g. Replace the a.c. power cord.

h. Place the ON/OFF switch on the Emulator to ON and proceed to Chapter 4, Operation.

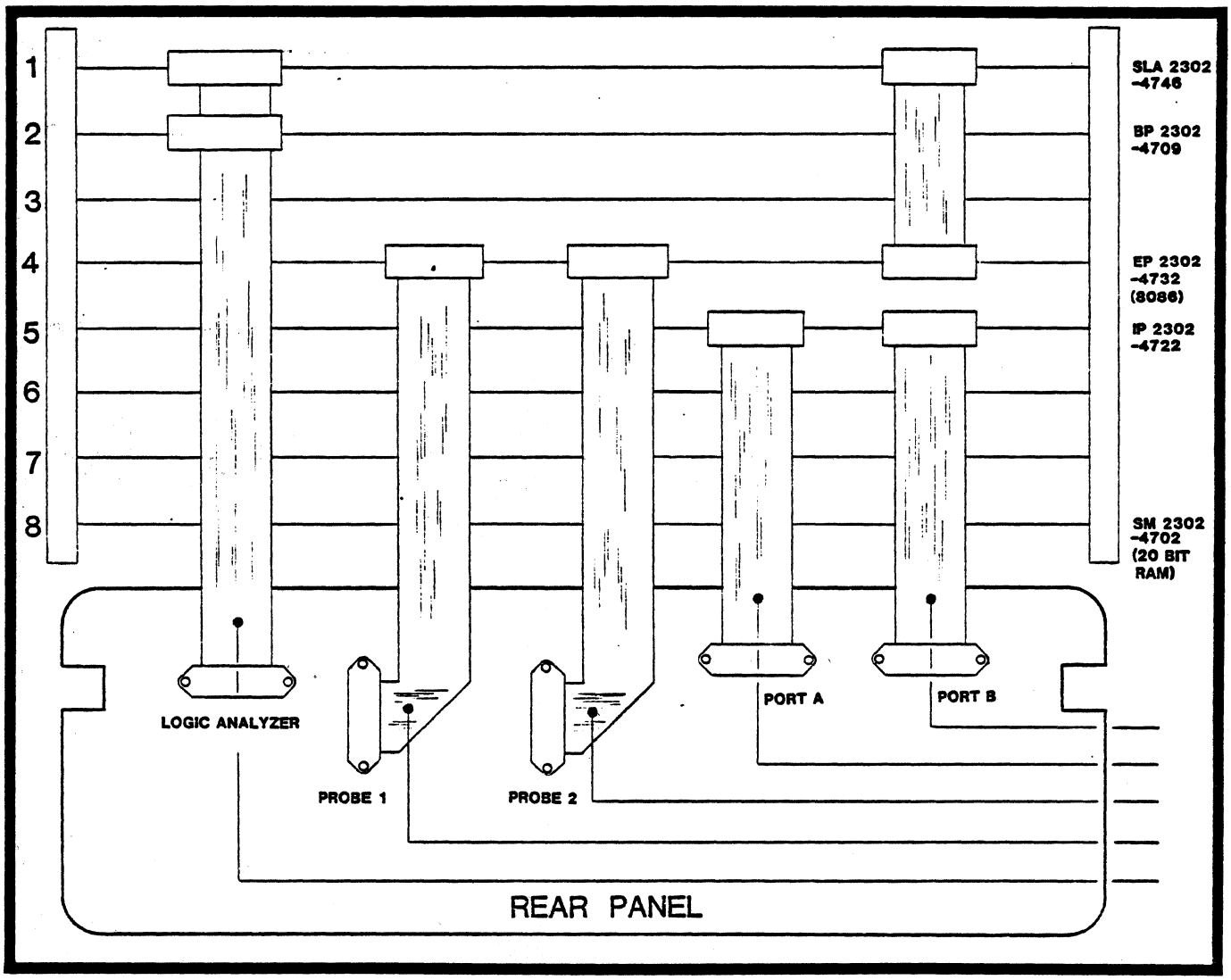


Figure 3-1. Slave Emulator (Rear View) With SLA Installed

CHAPTER 4

OPERATION

4.1 INTRODUCTION

The Slave Logic Analyzer (SLA) option allows the user to view the emulated processor's operation by displaying as many as 64 processor functions in three different formats. The user may record a trace of the target processor's activity in real time.

Parameters which the user can control include the following:

Trace qualifier	To identify a specific subset of bus cycles to trace. Breakpoint 3 serves as the trace qualifier.
Trigger event identity	Breakpoints 0, 1, and 2 may serve as a Logic Analyzer trigger.
Trace contents, relative to trigger event	A post-trigger delay count identifies how many qualified bus cycles to trace after the triggering event occurs.

The Logic Analyzer's trace buffer is large enough to trace 256 bus cycles. These actually represent target processor execution cycles, but the term "bus cycles" is used to suit common usage, whether or not the target processor is connected to a bus in the target system.

Event timing is another Logic Analyzer function. The Analyzer has a mode in which it times the interval between Breakpoints 1 and 2, allowing accurate measurement of the elapsed time between two events. Such an interval can be measured in microseconds, hundreds of nanoseconds, or bus cycles.

Software enhancements in the following functions provide support for the SLA:

Window mode command
Mode command
Breakpoint command
Qualify trace command

4.1.1 COMMAND DEFINITIONS

A definition of each of these commands is given here; a more detailed discussion follows in the section entitled **COMMANDS.**

WINDOW MODE COMMAND

The Window Mode command accepts three new modes. Each new mode selects one of the Logic Analyzer display formats listed below for the current window. It also allows the user to edit the set of signals to be shown by the waveform display.

Logic Analyzer trace data may be displayed in the following formats:

Cycle data	Each bus cycle is formatted on a single line, with most information shown in hexadecimal.
Waveform	Individual signals in the trace are drawn as lines in the display, as in a waveform diagram.
Execution trace	This processor-dependent display shows disassembled instructions combined with the data they manipulate on the target bus.

MODE COMMAND

The Mode command provides options for both breakpoint and Logic Analyzer functions. These controls are unified in a single command because the Logic Analyzer is actually an extension of breakpoint support.

BREAKPOINT COMMAND

The Breakpoint command itself is essentially unchanged, but the meaning of breakpoints is expanded when the Logic Analyzer is enabled.

QUALIFY TRACE COMMAND

The Qualify Trace command sets parameters to select bus cycles to be traced when the Analyzer is enabled. These parameters are identical to those used with breakpoints, but the meaning of a match condition is "trace this cycle" rather than "break execution". This command also sets the post-trigger delay, which indicates how many bus cycles to trace after the triggering event occurs.

4.2 GENERAL OPERATION

Using the Logic Analyzer requires defining a new emulation environment for the Slave Emulator and reconfiguring the ADS display. Since only wide windows are used for SLA displays, the user must invoke the Screen Map command and set the current window to a wide window display. The current window is indicated by a long reverse video line. <TAB> is used to redefine the current display window. Please refer to **SCREEN MAP HELP DISPLAY.**

The user must then invoke the Window Mode command to change the current window to one of the three Logic Analyzer modes; Cycle data, Waveform, or Execution Trace display. Please refer to the **WINDOW MODE COMMAND HELP DISPLAY.**

Initially, when the Logic Analyzer window option has been selected, the window displays the message ****no trace data available**.** Three additional steps are required to use the Analyzer.

First, enable the Logic Analyzer using the Mode command. The Mode command is used to define both breakpoint and Logic Analyzer options. When this command is entered, a help display showing the submodes and current status of the submodes appears on the screen. Please refer to the **MODE COMMAND HELP DISPLAY.**

Next, invoke the Qualify Trace command to qualify the trace parameters to be used by the SLA. When this command is entered, the screen shows a help display with the current trace qualifier and the trace qualifier options. The trace qualifier uses Breakpoint 3 to define which bus cycles will be recorded by the Logic Analyzer. The user may record all bus cycles or just those concerning a particular address, data, or other option.

In addition, the relative position of the trigger within the trace can be defined by the post-trigger delay. The delay count can be set between 1 and 255. If the count is 1, tracing will halt one qualified trace after the breakpoint is reached and the 254 events prior to the break, along with the cycle corresponding to the break, will be displayed if available. If the trace qualifier suppresses tracing of this cycle, the last qualified cycle before the break will be displayed.

If the count is 255, tracing will halt 255 qualified traces after the break and at most, 255 events after the break will be displayed. If the break occurs before this many cycles are traced after the last Execute command, the number of cycles displayed will be less. Please refer to the **QUALIFY TRACE COMMAND HELP DISPLAY.**

Next, define Breakpoint 0, 1, or 2 as a trigger (or triggers) for the Logic Analyzer. When all conditions are set, the Execute command may be given and the Logic Analyzer will be updated when a breakpoint is reached. Please refer to the **BREAKPOINT COMMAND HELP DISPLAY.**

4.3 DETAILS OF LOGIC ANALYZER OPERATION

When the Logic Analyzer is enabled via the Mode command, the Analyzer begins tracing target bus cycles at one of two times:

If the target processor is halted, tracing begins when a user's Execute command releases it to run.

If the target processor is running, tracing begins as soon as the Slave Emulator recognizes the mode change. The Slave Emulator halts the target processor while it changes Breakpoint/Logic Analyzer modes, then releases it to execute.

Once started, the Logic Analyzer examines each target cycle for a match with the trace qualifier. The trace buffer is circular, always keeping the 256 newest entries.

Tracing continues until a breakpoint occurs. The breakpoint serves only as a trigger signal when the Logic Analyzer is enabled; execution continues until the number of additional qualified cycles traced matches the user's post-trigger delay parameter. At that point, the Logic Analyzer freezes its trace buffer and the break occurs.

The Slave Emulator copies out the Logic Analyzer's trace buffer and notifies the ADS as soon as possible after the execution break. The ADS displays the appropriate **Stopped at breakpoint** or **Running, snapshot at breakpoint** message and updates any Logic Analyzer data in the display from the new trace contents.

The Logic Analyzer always traces at least one bus cycle after the trigger. The post-trigger delay must be in the range of 1 to 255. Logic Analyzer displays assign consecutive entry numbers to the traced bus cycles. Each entry number is a signed two-digit hexadecimal value which represents the cycle's age relative to the triggering cycle. Entry +00 is always the triggering cycle. If the trace qualifier prohibits tracing of the triggering bus cycle, entry +00 corresponds to the last qualified cycle which precedes the triggering event.

The trace qualifier is implemented by the same hardware which implements Breakpoint 3. Thus, while the Analyzer is enabled, only three breakpoints are available. During this time, the user is free to set parameters for breakpoint 3, but they will be ignored until the user disables the Analyzer via the Mode command.

Whenever the user issues a command which affects the enabled/disabled state of the Logic Analyzer or sets Breakpoint 3 with the Logic Analyzer enabled, the Slave Emulator Debugger displays one of the following two messages:

******Analyzer enabled, break 3 disabled******
******Analyzer disabled, break 3 enabled******

Normally, the execution break stops the target processor, but the user has two controls to alter this:

If the breakpoint is a snapshot, the Slave Emulator normally halts the target system while it retrieves the contents of its hardware trace buffer. Using the Mode command, the user may set the "run/pause after trace" mode to "run", rather than the default ("pause"). The target processor continues running at the expense of missing target bus cycles until the trace buffer has been copied.

If the breakpoint is a snapshot, the Slave Emulator also checks the "scope" mode. Scope settings are:

0	Keeps a snapshot breakpoint from interfering with target execution at all.
1	Interrupts target execution long enough to get a snapshot of register contents.
2	Interrupts target execution for a longer period to snap both registers and memory.

If "run/pause after trace" is set to "run" and "scope" is set to "0", snapshot breakpoints never interrupt target system execution. Instead they trigger updates of the Logic Analyzer trace.

Event Timing

When all breakpoint and Logic Analyzer modes are set for event timing, Breakpoint 1 starts a 24-bit counter in the Logic Analyzer. The maximum value of the counter is 16,777,216 (decimal); if the count exceeds that value, the counter starts at zero again.

This counter increments at one of three rates:

once per microsecond
once per 100 nanoseconds
once per target bus cycle

The user may select the desired rate via the Mode command.

When Breakpoint 2 occurs, the counter stops. The Slave Emulator Debugger translates the value of this counter into decimal and displays a message. For example:

******Elapsed time 75 μsec******

For other timer modes, the unit identification changes accordingly. Note that times clocked in hundreds of nanoseconds are reported in nanoseconds in order to simplify the text which identifies the timer units. Thus, the nanosecond equivalent of the 75 microsecond interval in the example above might appear as:

******Elapsed time 75200 nanosec******

The time interval reported in this instance is accurate to three significant digits, rather than to five.

The event timing function also uses Breakpoint 2 as a normal trigger for Logic Analyzer tracing.

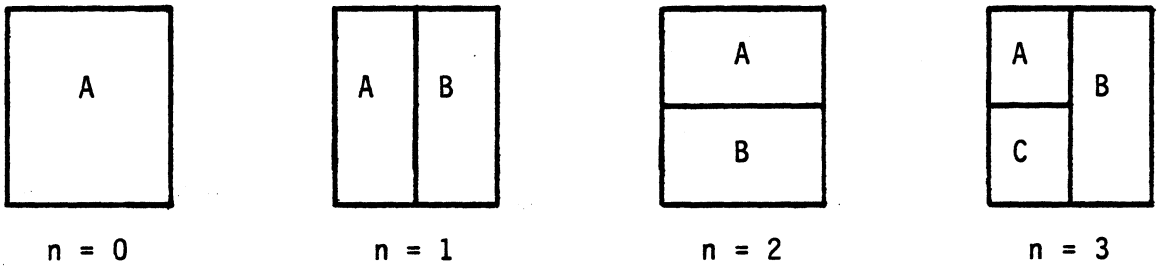
For further information regarding the use of the Slave Emulator in general, please refer to the GenRad/DSD **Slave Emulator Reference Manual**, (2302-5000-00).

4.4 COMMANDS

SCREEN MAP COMMAND

HELP DISPLAY

Screen map n maps up to four display windows onto the screen, with windows assigned to quadrants of the display as shown below.
Windows are labelled A - D.



Any of the eight screen maps may be selected for viewing target memory. n specifies the desired map, as shown in the help display. The default screen map is n = 2. Each window may display symbolic (disassembled) or hexadecimal/ASCII memory data, or Logic Analyzer trace data in any of three formats. Logic Analyzer trace data can only appear in a window which spans the full width of the screen.

If the current window is the incorrect size to support Logic Analyzer data, an error message stating **XXX Requires wide window** will be displayed and the command aborted. This error message may be issued by both the Screen map command and the Window mode command.

4.4.1 WINDOW MODE COMMAND

HELP DISPLAY

Window Mode command operands:

Symbolic	Display memory data as disassembled symbolic instructions.
Hex	Display memory data as hexadecimal bytes and ASCII characters.
Cycle data	Display raw (minimally formatted) Logic Analyzer trace data.
Waveform	Display signals as waveforms from Logic Analyzer trace data.
Execution	Display execution trace from Logic Analyzer trace data.
Absolute	Use absolute addresses, referencing entire target address space.
Offset	Use 16-bit offset addresses, referencing a 64K segment beginning at the window's offset base address.

**Absolute/offset mode applies to memory displays, not to Analyzer traces.

Window modes fall into three groups:

Memory display modes	Symbolic, hex
Logic Analyzer display modes	Cycle data, waveform, execution
Memory display modifiers	Absolute, offset

All modes in the first two groups are mutually exclusive. Selecting any one of them automatically resets the old mode. The memory display modifiers can be set independently, but they are only meaningful in connection with symbolic or hex memory display modes.

The command terminates after the user confirms his choice of any mode except "waveform". When the user confirms the waveform mode setting, the mode command establishes a default signal mapping for the current window and a dialog function which allows the user to edit this mapping.

Waveform Display

This display presents the state of the individual target processor signals as a function of time. This defines a waveform for each signal, but the waveform is limited in two ways:

Each signal is represented as being purely binary: it is either high or low. This corresponds to the way in which typical digital logic perceives the signal, but it does not offer clues to noisy or floating signals.

The waveform is generated by sampling data at the pins of the target processor chip once per cycle and drawing lines to connect these points. This technique does not detect fine details of signal transitions which occur within a cycle.

The signal map contains positions for up to 64 signals from the target processor (numbered 0-63). The default map assigns the set of lines being traced to consecutive positions in the map.

The initial display for the map-editing dialog appears as follows for a 6809 Emulator:

Enter trace position, RETURN, TAB, or "?":

Signal mapping (trace position, signal name pairs):

0	A0	8	A8	16	D0	24	RD/WR-	32	MRDY	40		48		56	
1	A1	9	A9	17	D1	25	FIRQ-	33	OPFTCH-	41		49		57	
2	A2	10	A10	18	D2	26	NMI-	34	BREQ-	42		50		58	
3	A3	11	A11	19	D3	27	RESET-	35	EC0	43		51		59	
4	A4	12	A12	20	D4	28	BA	36	EC1	44		52		60	
5	A5	13	A13	21	D5	29	BS	37	EC2	45		53		61	
6	A6	14	A14	22	D6	30	IRQ-	38	EC3	46		54		62	
7	A7	15	A15	23	D7	31	HALT-	39		47		55		63	

Available signals:

A0	A1	A2	A3	A4	A5	A6	A7
A8	A9	A10	A11	A12	A13	A14	A15
D0	D1	D2	D3	D4	D5	D6	D7
RD/WR-	FIRQ-	NMI-	RESET-	BA	BS	IRQ-	HALT-
MRDY	OPFTCH-	BREQ-	EC0	EC1	EC2	EC3	

The top portion of the screen shows the entire signal map, and the bottom portion shows the entire set of signals available for display.

The available signals fall into the following groups:

A0-An	Address lines. The number of these lines depends on the target processor.
D0-Dn	Data lines. The number depends on the target processor.
Processor-dependent signals	These miscellaneous signals bear names as similar as possible to those used by the chip manufacturer.
EC0-EC3	External connections. These may be connected to any signals in the user's target system.

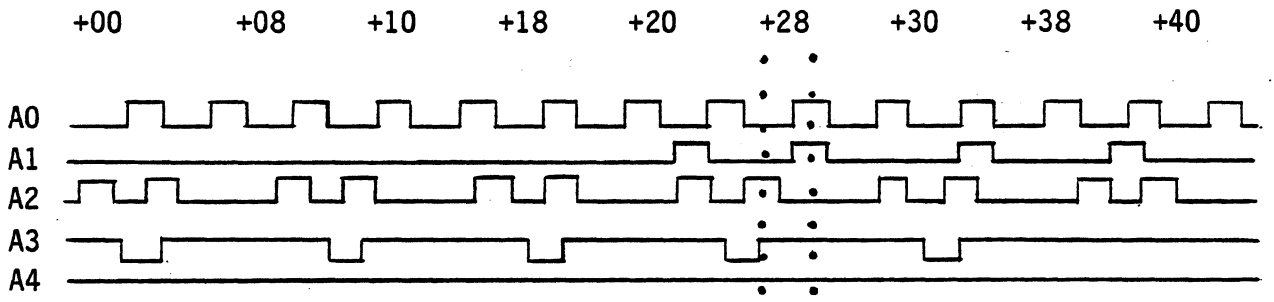
Enter the trace position, <RETURN>, <TAB>, or <?>.

Trace position	Identify the position within the map which is to be set. The trace position is a decimal integer 0-63.
<RETURN>	Accept signal map as displayed and terminate command.
<TAB>	Set entire map to its default and resume dialog.
<?>	Generates the help display.

The ADS prompts for a signal name or <RETURN> after the user enters a trace position. <RETURN> specifies that no signal is to be mapped in this trace position; the corresponding line in a waveform display is blank. A signal name is completed automatically when the user enters enough characters to uniquely identify it to the system. The ADS asks for confirmation and sets the previously selected map position to show this signal.

The display itself shows one signal per line in its window and uses special graphic characters to draw transitions between high and low states.

The example below shows a waveform display shown on a screen that may also contain symbolic or hex data. Only five lines (A0 - A4) are shown. If the screen was mapped to a single window, thirteen lines (A0 - A12) would be shown.



Labels across the top of the display identify trace entry numbers at intervals of eight entries. The current entry's position is approximately in the center of the data, and signals within the current entry fall within a vertical reverse-video bar.

Signal names appear to the left of the traces. These names can be edited in the Window Mode command to group signals in any order, to delete signals from the set to be displayed, to add signals to the set to be displayed, and to supply blank lines between groups of signals.

As in the cycle data display, the Display command and related functions assign values to the current entry to position the display over any part of the trace data. One subtle difference is that the up and down arrow keys position new sets of signals in the window, rather than positioning a new set of entries.

The number of signals which can be displayed at one time is generally much less than the number of signals for which trace data are saved. By using up and down arrows it is possible to roll vertically through the entire set of signals available for display.

The following table shows the association of processor-dependent data bits with particular signals for each target processor. Signal names shown below are those which would appear in a Logic Analyzer waveform display. Blank slots indicate bits which are not used, or which are only used internally by the Slave Emulator:

Bit #	Bit pattern	8086	68000	6809	6502
0	1 0 0 0 0				
1	2 0 0 0 0	RD/WR-	RD/WR-	RD/WR-	RD/WR-
2	4 0 0 0 0	I/O		OPFTCH-	
3	8 0 0 0 0	BHE			
4	0 1 0 0 0		UDS-	FIRQ-	SYNC
5	0 2 0 0 0	S0-	LDS-	NMI-	
6	0 4 0 0 0	S1-	FC0	RESET-	
7	0 8 0 0 0	S2-	BGACK		RDY
8	0 0 1 0 0		FC1-		IRQ-
9	0 0 2 0 0		FC2-		NMI-
10	0 0 4 0 0		HALT-	BA	RES-
11	0 0 8 0 0	QT1			
12	0 0 0 1 0	QT2		BS	
13	0 0 0 2 0	QT3	BG-	IRQ-	
14	0 0 0 4 0	RD-	IPL0-	HALT-	
15	0 0 0 8 0	INTA-	IPL1-	MRDY	
16	0 0 0 0 1	NMI			
17	0 0 0 0 2	INT	IPL2-		
18	0 0 0 0 4	RESET	BERR-		
19	0 0 0 0 8	HLDACK-	BR-	BREQ-	

Cycle Data Display

Each entry in this display presents all recorded data for a single bus cycle. Entries are formatted on separate lines, with cycle data grouped into columns, as shown in the following sample display from a 6809 emulator:

	Operation	Addr	Data	Ext lines	Processor-dependent
-05	Write memory	E710	00	1111	5 7 2 C E
-04	Write memory	E711	00	1111	D 7 2 C E
-03	Opcode fetch	E42F	8E	1111	3 7 0 C 8
-02	Read memory	E43F	E4	1111	F 7 0 C C
-01	Read memory	E431	3D	1111	7 7 0 C C
+00	**Opcode fetch**	**E431**	**BF**	**1111**	**B 7 0 C 8**
+01	Read memory	E433	E7	1111	7 7 0 C C
+02	Read memory	E4FF	00	1111	F 7 0 C C
+03	**Read memory**	**FFFF**	**55**	**1111**	**F 7 0 C C**
+04	Write memory	E700	E4	1111	5 7 2 C E
+05	Write memory	E701	3D	1111	D 7 2 C E
+06	Opcode fetch	E435	7E	1111	3 7 0 C 8
+07	Read memory	E435	F3	1111	F 7 0 C C
+08	Read memory	E4FF	07	1111	7 7 0 C C

Entry +03 appears in reverse video in the actual display to indicate that it is the current entry in the current window. Entry +00, the bus cycle that triggered the breakpoint, is displayed in double intensity in the actual display.

The sample display above was generated with Screen Map 0 selected, so that the entire data portion of the display is devoted to this window. The cycle data display may also be used with other screen maps so that it occupies either the top or bottom half of the data display. In either case, the current entry is centered vertically within the window. In the sample above, the user specified a post-trigger delay of 8 and selected a current entry which is close to the end of the trace data, so that a few lines below entry +08 are blank.

Display data is defined as follows:

Entry number:	The signed two-digit hexadecimal value in the leftmost column shows the position of each entry relative to the triggering bus cycle. The user can center the window's display around any particular entry by using the Display command to select that entry as current. The current address set by the display command is simply taken to be the current entry. Use of signed values for entry numbers requires that the user enter "Display 0-n" to display entry "-n". "Display -n" uses the usual defaulting technique to display entry "c-n", where "c" is the number of the current entry. The arrow keys and the "+" and "-" commands change the current entry number in the same way as they do for memory addresses.
Operation:	The ASCII name identifying the type of bus cycle indicated by this trace entry. The cycle identification is derived from processor-dependent data in the trace entry.
Addr:	The hexadecimal address present on the processor's address bus during the cycle. The address is reported as if all bits on the target address bus are meaningful; in actual practice, some types of cycles on some processors do not use the entire width of the address bus.
Data:	The hexadecimal data communicated in this cycle. The cycle data display uses processor-dependent bits to determine how much data is meaningful for each cycle, and formats only the appropriate part of the data bus.
Ext lines:	This represents the four external lines which the user may connect to any signal in the target system. The values of these lines are shown in binary, with Line 0 regarded as the low-order rightmost bit and Line 3 regarded as the high-order leftmost bit. The external lines display 1111 when the probes are not connected.
Processor-dependent:	This column shows 20 bits of data formatted as individual hex digits, which have unique meanings for each processor. These typically include bits which define the type of cycle, indicate processor status, report pending interrupt requests, etc. These signals are numbered from 0-19 for identification purposes. The leftmost hex digit contains signals 0-3, with 0 in the low-order (rightmost) bit position within the digit. Each successive digit to the right contains the next higher-numbered four bits in the same bit order.

4.4.2 MODE COMMAND

The Mode command uses a display format and user dialog similar to those used by the breakpoint command. The sample display below incorporates current mode settings which correspond to the initial defaults except for the enable/disable Analyzer submode:

HELP DISPLAY

Mode parameter:

******Analyzer enabled, break 3 disabled******

```
-----------------------------------------+-----------------------------------------
                                         |
Mode                                     |Breakpoint/logic analyzer modes
                                         |
    and/or breaks = A or O               |    And/or breaks = O
    scope = [scope]                      |    Scope = 1 (snap regs only)
    enable/disable analyzer = E or D     |    Enable/disable analyzer = E
    run/pause after trace = R or P       |    Run/pause after trace = P
    timer units = [unit code]            |    Timer units = microseconds
                                         +-----------------------------------------
    Default all mode parameters to inital values.
    Set all mode parameters for event timing.

-------------------------------------------------------------------------------

[scope]       Scope of information updated at a snapshot breakpoint:
                   0 = Nothing
                   1 = Register contents
                   2 = Register contents and memory being displayed
      **Logic Analyzer trace is independent of snapshot breakpoint scope

[unit-code]   Units used by event timer:
                   Microseconds
                   Nanoseconds (min. resolution = 100 nanoseconds)
                   Bus cycles

-------------------------------------------------------------------------------
```

AND/OR breaks mode specifies how different breakpoints interract:

OR indicates all breakpoints function independently.

AND indicates all breakpoints function together. Initially only the lowest-numbered active breakpoint is armed; when its conditions are satisfied it arms the next higher-numbered breakpoint, rather than causing an actual break. The break finally occurs when the highest-numbered active breakpoint's conditions are satisfied.

Scope indicates how much data the Slave Emulator updates when the target system reaches a snapshot breakpoint:

0 = Nothing	The Slave Emulator does not interrupt the target system and does not report register or memory contents to the ADS. This is useful only when the breakpoints are used to trigger the Logic Analyzer while the target system continues running in full-speed emulation.
1 = Register contents	The Slave Emulator interrupts the target system for about 10 milliseconds to examine the current register contents and reports these to the ADS.
2 = Register contents and memory displayed	The Slave Emulator interrupts the target system for about 100 milliseconds to examine the current register contents and check for altered data in memory areas whose contents are buffered in the ADS for the Debugger display.

In the display of current mode settings this parameter appears as:

0 (snap nothing)
1 (snap regs only)
2 (snap regs and mem)

Enable/disable Analyzer enables or disables Logic Analyzer operation and breakpoint 3. In this mode, reaching a breakpoint (either ORed or ANDed) supplies a Logic Analyzer trace trigger. Execution continues until the number of bus cycles indicated by the post-trigger delay has been traced.

Run/pause after trace specifies whether or not the target processor is to continue running while the Slave Emulator copies out the contents of the Logic Analyzer's trace buffer. This applies only when the triggering breakpoint specifies the "snap" option.

The run setting allows the target processor to continue execution. If the snapshot scope mode is 0 this causes Logic Analyzer trace updates with absolutely no interruption of target system execution. Other settings of the snapshot scope mode delay the target system by the times quoted above. The penalty for this mode is that breakpoints and Logic Analyzer tracing must remain disabled while the Slave Emulator copies the trace buffer. The target system may miss breakpoints.

The pause setting halts the target system while the Slave Emulator copies the Logic Analyzer trace buffer. This insures that breakpoints cannot be missed and that all target system execution is traced, but it suspends target execution for a longer time interval than that needed to satisfy the breakpoint scope mode.

The timer units mode indicates what unit the Logic Analyzer's event timer uses. The **event timer** is active only when the following modes are in effect:

```
And/or breaks = A
Scope = 0 (snap nothing)
Enable/disable analyzer = E
Run/pause after trace = R
```

This combination of modes causes the emulator to force all breakpoints to be snapshots.

Under these conditions the event timer begins clocking real time or bus cycles when the conditions for Breakpoint 1 are satisfied and stops when Breakpoint 2 triggers the Logic Analyzer. Breakpoint 0 has no effect on the event timer.

The event timer uses a 24-bit counter in one of three modes:

Microseconds	Counter increments once per microsecond; elapsed interval reported in microseconds.
Nanoseconds	Counter increments once per 100 nanoseconds; elapsed interval reported in nanoseconds.
Bus cycles	Counter increments once per target system bus cycle; elapsed interval reported as bus cycle count.

The elapsed time or bus cycle counts observed by the event timer are reported to the user in the ADS display's message area, instead of the usual message **Running, snapshot at break 2.** "Default all mode parameters to initial values" sets all parameters to the standard value in effect when the Slave Emulator is reset. These settings are:

```
And/or breaks = 0
Scope = 1 (snap regs only)
Enable/disable analyzer = D
Run/pause after trace = P
Timer units = microseconds
```

The user must confirm to accomplish this mode change.

"Set all mode parameters for event timing" sets the parameters to the values defined under event timer in order to activate the event timer and sets the timer units to microseconds. The user must confirm to accomplish this mode change.

4.4.3 BREAKPOINT COMMAND

HELP DISPLAY

```
breakpoint (0-3) n  (delim)
    count = [dec]
    address = [abs]
    data = [data]
    external lines = [bin4]
    instruction/data = I, D, or X
    read/write = R, W, or X
    memory/io = M, I, or X
    halt/snap = H or S
```

```
Breakpoint 2
     Count = 1
     Address = FF39E
     Data = XXXX
     External lines = XXXX
     Instruction/data = I
     Read/write = R
     Memory/io = M
     Halt/snap = H
```

```
[delim]  ,=> edit parameters, other => set execution breakpoint
n        Breakpoint number:  0-3
[dec]    Decimal repetition count:  1-32767
[abs]    Expression or up to 6 hex digits, X for "don't care" digit
[data]   Expression or up to 4 hex digits, X for "don't care" digit
[bin4]   4 binary digits, X for "don't care" digit
```

Use of breakpoints as Logic Analyzer triggers is described in the section entitled **GENERAL OPERATION.** Aside from triggering the Logic Analyzer, breakpoints change their apparent behavior in two specific ways when the Analyzer is enabled:

The execution break is delayed by the number of cycles specified in the trace qualifier's post-trigger delay. A variable number of instructions may be executed after the break conditions are satisfied.

When all modes are set for event timing, the ANDed breakpoints behave as snapshots, even though Breakpoint 2 specifies that execution be halted.

4.4.4 QUALIFY TRACE COMMAND

Qualify trace functions exactly as the breakpoint command, except that the parameters it sets are those of the Logic Analyzer's trace qualifiers (Breakpoint 3).

HELP DISPLAY

Qualifier parameter:

******Logic analyzer disabled ******

qualify trace post-trigger delay = [dec] address = [abs] data = [data] external lines = [bin4] instruction/data = I, D, or X read/write = R, W, or X memory/io = M, I, or X	Trace qualifier Post-trigger delay = 1 Address = XXXXXX Data = XXXX External lines = XXXX Instruction/data = X Read/write = X Memory/io = X

[dec]	Decimal bus cycle count: 1-255
[abs]	Expression of up to 6 hex digits, X for "don't care" digit.
[data]	Expression of up to 4 hex digits, X for "don't care" digit.
[bin4]	Four binary digits, X for "don't care" digit.

Trace qualifier parameters are:

Post-trigger delay:	Number of bus cycles to trace after a trigger (after a breakpoint). This is a decimal number 1-255 with the default being 1.
Address:	Address pattern to trace. This is a hexadecimal number in which "X" in any digit indicates "don't care". The number of digits in this number depends on the width of the target processor's address bus. The default is entirely "don't care" digits.
Data:	Data pattern to trace. This is a hexadecimal number in which "X" in any digit indicates "don't care". The number of digits in this number depends on the width of the target processor's data bus. The default is entirely "don't care" digits.

External lines:	External line values to trace. This number consists of four binary digits in which "X" in any digit indicates "don't care". The default is entirely "don't care" digits.
Instruction/data:	
I	Trace only opcode or instruction-fetch cycles.
D	Trace only data access cycles. Most processors do not distinguish between operand fetches and fetches for the second and subsequent bytes or words of instructions.
X	Default; means trace both instruction fetches and data accesses.
Read/write:	
R	Trace only read cycles.
W	Trace only write cycles.
X	Trace both read and write cycles.
Memory/IO:	
M	Trace only cycles which access memory.
I	Trace only cycles which access I/O ports.
X	Default; trace both memory and I/O accesses.

The memory/IO parameter is ignored for processors that do not have a separate I/O address space.

The trace qualifier enables tracing of all bus cycles when all of its parameters have the default "don't care" setting.

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